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Requester's Full Name: P. Laufer Examiner#: 73139 Date: 6/13/02  
Art Unit: \_\_\_\_\_ Phone Number: 30 Serial Number: 101066475  
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\*\*\*\*\*  
Please provide a detailed statement of the search topic, and describe as specifically as possible the subject matter to be searched. Include the elected species or structures, keywords, synonyms, acronyms, and registry numbers, and combine with the concept or utility of the invention. Define any terms that may have a special meaning. Give examples or relevant citations, authors, etc., if known. Please attach a copy of the cover sheet, pertinent claims, and abstract.

Title of Invention: \_\_\_\_\_

Inventors (please provide full names): \_\_\_\_\_

Earliest Priority Filing Date: \_\_\_\_\_

*\*For Sequence Searches Only\* Please include all pertinent information (parent, child, divisional, or issued patent numbers) along with the appropriate serial number.*

Litigation  
6,021,265

06-13-02 P05:16 IN

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Searcher: <u>S Green</u>	NA Sequence (#) _____	<u>STN</u>
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Clerical Prep Time: _____	Patent Family _____	<u>WWW/Internet</u>
Online Time: <u>10</u>	Other _____	Other (specify) _____

1 of 1 DOCUMENT

6,021,265

GET 1st DRAWING SHEET OF 3

Feb. 1, 2000

Interoperability with multiple instruction sets

REISSUE: Reissue Application filed Feb. 1, 2002 (O.G. May 14, 2002) Ex.  
Gp.: 2758; Re. S.N. 10/066,475

INVENTOR: Nevill, Edward Colles, Cambridge, United Kingdom

ASSIGNEE-AT-ISSUE: ARM Limited, Cambridge, United Kingdom (03)

APPL-NO: 840,557

FILED: Apr. 14, 1997

FOR-PRIOR:

Jun. 10, 1994 United Kingdom 9411670

REL-US-DATA:

Division of Application No. 8-477,781, Jun. 7, 1995 now patented  
5,758,115

INT-CL: [6] G06F 9#30

US-CL: 395#385; 395#386

SEARCH-FLD: 395#384, 385, 386

PRIM-EXMR: Harrell, Robert B.

ASST-EXMR: Coulter, Kenneth R.

LEGAL-REP: Fenwick & West LLP

PARCASE: RELATED APPLICATIONS

This is a divisional of application Ser. No. 08/477,781 filed on  
Jun. 7, 1995 now U.S. Pat. No. 5,758,115.

**LEXIS-NEXIS**  
**Library: PATENT**  
**File: ALL**

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**LEXIS-NEXIS**  
**Library: PATENT**  
**File: CASES**

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**LEXIS-NEXIS**  
**Library: PATENT**  
**File: JNLS**

?us6021265/pn

\*\* SS 4: Results 1

Search statement 5

?prt full nonstop legalall

1/1 PLUSPAT - (C) QUESTEL-ORBIT

PN - US6021265 A 20000201 [US6021265]

TI - (A) Interoperability with multiple instruction sets

PA - (A) ADVANCED RISC MACH LTD (GB)

IN - (A) NEVILL EDWARD COLLES (GB)

AP - US84055797 19970414 [1997US-0840557]

PR - US84055797 19970414 [1997US-0840557]

- GB9411670 19940610 [1994GB-0011670]

- US47778195 19950607 [1995US-0477781]

IC - (A) G06F-009/30

EC - G06F-009/318

PCL - ORIGINAL (O) : 712209000; CROSS-REFERENCE (X) : 712210000

DT - Basic

CT - US4274138; US4338663; US4839797; US4876639; US5193158; US5327566;

US5392408; US5404472; US5420992; US5475824; US5481684; US5481693;

US5524211; US5568646; US5574928; US5598546; US5638525; US5758115;

EP0109567; EP0169565 A; EP0199173; EP0306920 A2; EP0324308 A2;

JP58-3040; GB2016755 A; GB20167550 A

- IBM Technical Disclosure Bulletin by P. F. Smith, entitled: "Extended Control for Microprocessors" vol.17 No.11 published Apr. 1975, pp. 3438-3441.

IBM Technical Disclosure Bulletin entitled: "Oncode Remap and Compression in Hard-Wired Risc Microprocessor" vol. 32 No. 10A published Mar. 1990, p. 349.

IBM Technical Disclosure Bulletin by J. C. Kemp, entitled: "Instruction Translator" vol. 15 No. 3 published Aug. 1972, p. 920.

STG - (A) United States patent

AB - Data processing apparatus comprising: a processor core having means for executing successive program instruction words of a predetermined plurality of instruction sets; a data memory for storing program instruction words to be executed; a program counter register for indicating the address of a next program instruction word in the data memory; means for modifying the contents of the program counter register in response to a current program instruction word; and control means, responsive to one or more predetermined indicator bits of the program counter register, for controlling the processor core to execute program instruction words of a current instruction set selected from the predetermined plurality of instruction sets and specified by the state of the one or more indicator bits of the program counter register.

1/1 LGST - (C) LEGSTAT

PN - US 6021265 [US6021265]

AP - US 840557/97 19970414 [1997US-0840557]

DT - US-P

ACT - 19970414 US/AE-A

APPLICATION DATA (PATENT)

{US 840557/97 19970414 [1997US-0840557]}

- 20000201 US/A

PATENT

- 20020514 US/RF  
REISSUE APPLICATION FILED  
20020201  
UP - 2002-22

1/1 CRXX - (C) CLAIMS/RRX  
PN - 6,021,265 A 20000201 [US6021265]  
PA - ARM Ltd GB  
ACT - 20020201 REISSUE REQUESTED  
ISSUE DATE OF O.G.: 20020514  
REISSUE REQUEST NUMBER: 10/066475  
EXAMINATION GROUP RESPONSIBLE FOR REISSUEPROCESS: 2758

Reissue Patent Number:

1/1 PAST - (C) Thomson Derwent  
AN - 200220-001734  
PN - 6021265 A [US6021265]  
OG - 2002-05-14  
ACT - REISSUE APPLICATION FILED

fam us6021265/pn

1 Patent Groups  
\*\* SS 4: Results 9

Search statement 5

?famstate nonstop

1/9 INPADOC - (C) INPADOC

PN - GB 9411670 A0 19940803 [GB9411670]  
TI - INTEROPERABILITY WITH MULTIPLE INSTRUCTION SETS  
PA - ADVANCED RISC MACH LTD  
AP - GB 9411670/94-A 19940610 [1994GB-0011670]  
PR - GB 9411670/94-A 19940610 [1994GB-0011670]

2/9 INPADOC - (C) INPADOC

PN - GB 2290395 A1 19951220 [GB2290395]  
TI - INTEROPERABILITY WITH MULTIPLE INSTRUCTION SETS  
IN - NEVILL EDWARD COLLES  
PA - ADVANCED RISC MACH LTD [GB]  
AP - GB 9411670/94-A 19940610 [1994GB-0011670]  
PR - GB 9411670/94-A 19940610 [1994GB-0011670]  
IC - G06F-009/30

1/1 LEGALI - (C) LEGSTAT

PN - GB 2290395 [GB2290395]  
AP - GB 9411670/94 19940610 [1994GB-0011670]  
DT - GB-P  
ACTE- 19940610 GB/AE-A  
APPLICATION DATA  
{GB 9411670/94 19940610 [1994GB-0011670]}  
- 19951220 GB/A1  
APPLICATION PUBLISHED  
- 19970528 GB/B2 [+]  
PATENT GRANTED  
UP - 1997-35

3/9 INPADOC - (C) INPADOC

PN - GB 9702595 A0 19970326 [GB9702595]  
TI - INTEROPERABILITY WITH MULTIPLE INSTRUCTION SETS  
PA - ADVANCED RISC MACH LTD  
AP - GB 9702595/97-A 19940610 [1997GB-0002595]  
PR - GB 9702595/97-A 19940610 [1997GB-0002595]  
- GB 9411670/94-A3 19940610 [1994GB-0011670]

4/9 INPADOC - (C) INPADOC

PN - GB 2307072 A1 19970514 [GB2307072]  
TI - INTEROPERABILITY WITH MULTIPLE INSTRUCTION SETS  
IN - NEVILL EDWARD COLLES  
PA - ADVANCED RISC MACH LTD [GB]  
AP - GB 9702595/97-A 19940610 [1997GB-0002595]  
PR - GB 9702595/97-A 19940610 [1997GB-0002595]  
- GB 9411670/94-A3 19940610 [1994GB-0011670]  
IC - G06F-009/30

1/1 LEGALI - (C) LEGSTAT  
PN - GB 2307072 [GB2307072]  
AP - GB 9702595/97 19940610 [1997GB-0002595]  
DT - GB-P  
ACTE- 19940610 GB/AE-A  
APPLICATION DATA  
{GB 9702595/97 19940610 [1997GB-0002595]}  
- 19970514 GB/A1  
APPLICATION PUBLISHED  
- 19980513 GB/B2 [+]  
PATENT GRANTED  
UP - 1998-20

5/9 INPADOC - (C) INPADOC  
PN - GB 2290395 B2 19970528 [GB2290395]  
TI - INTEROPERABILITY WITH MULTIPLE INSTRUCTION SETS  
IN - NEVILL EDWARD COLLES  
PA - ADVANCED RISC MACH LTD [GB]  
AP - GB 9411670/94-A 19940610 [1994GB-0011670]  
PR - GB 9411670/94-A 19940610 [1994GB-0011670]  
IC - G06F-009/30

1/1 LEGALI - (C) LEGSTAT  
PN - GB 2290395 [GB2290395]  
AP - GB 9411670/94 19940610 [1994GB-0011670]  
DT - GB-P  
ACTE- 19940610 GB/AE-A  
APPLICATION DATA  
{GB 9411670/94 19940610 [1994GB-0011670]}  
- 19951220 GB/A1  
APPLICATION PUBLISHED  
- 19970528 GB/B2 [+]  
PATENT GRANTED  
UP - 1997-35

6/9 INPADOC - (C) INPADOC  
PN - GB 2307072 B2 19980513 [GB2307072]  
TI - INTEROPERABILITY WITH MULTIPLE INSTRUCTION SETS  
IN - NEVILL EDWARD COLLES  
PA - ADVANCED RISC MACH LTD [GB]  
AP - GB 9702595/97-A 19940610 [1997GB-0002595]  
PR - GB 9702595/97-A 19940610 [1997GB-0002595]  
- GB 9411670/94-A3 19940610 [1994GB-0011670]  
IC - G06F-009/30

1/1 LEGALI - (C) LEGSTAT  
PN - GB 2307072 [GB2307072]  
AP - GB 9702595/97 19940610 [1997GB-0002595]  
DT - GB-P  
ACTE- 19940610 GB/AE-A  
APPLICATION DATA  
{GB 9702595/97 19940610 [1997GB-0002595]}  
- 19970514 GB/A1  
APPLICATION PUBLISHED  
- 19980513 GB/B2 [+]  
PATENT GRANTED  
UP - 1998-20



7/9 INPADOC - (C) INPADOC  
PN - JP 8044557 A2 19960216 [JP08044557]  
TI - DATA PROCESSOR  
IN - EDOWAADO KORESU NEBIRU  
PA - ADVANCED RISC MACH LTD  
AP - JP 143544/95-A 19950609 [1995JP-0143544]  
PR - GB 9411670/94-A 19940610 [1994GB-0011670]  
IC - G06F-009/30

8/9 INPADOC - (C) INPADOC  
PN - US 6021265 A 20000201 [US6021265]  
TI - INTEROPERABILITY WITH MULTIPLE INSTRUCTION SETS  
IN - NEVILL EDWARD COLLES [GB]  
PA - ADVANCED RISC MACH LTD [GB]  
AP - US 840557/97-A 19970414 [1997US-0840557]  
PR - US 840557/97-A 19970414 [1997US-0840557]  
- GB 9411670/94-A 19940610 [1994GB-0011670]  
- US 477781/95-A3 19950607 [1995US-0477781]  
IC - G06F-009/30

1/1 LEGALI - (C) LEGSTAT  
PN - US 6021265 [US6021265]  
AP - US 840557/97 19970414 [1997US-0840557]  
DT - US-P  
ACTE- 19970414 US/AE-A  
APPLICATION DATA (PATENT)  
{US 840557/97 19970414 [1997US-0840557]}  
- 20000201 US/A  
PATENT  
- 20020514 US/RF  
REISSUE APPLICATION FILED  
20020201  
UP - 2002-22

9/9 INPADOC - (C) INPADOC  
PN - US 5758115 A 19980526 [US5758115]  
TI - INTEROPERABILITY WITH MULTIPLE INSTRUCTION SETS  
IN - NEVILL EDWARD COLLES [GB]  
PA - NEVILL EDWARD COLLES [GB]  
AP - US 477781/95-A 19950607 [1995US-0477781]  
PR - GB 9411670/94-A 19940610 [1994GB-0011670]  
IC - G06F-009/30

1/1 LEGALI - (C) LEGSTAT  
PN - US 5758115 [US5758115]  
AP - US 477781/95 19950607 [1995US-0477781]  
DT - US-P  
ACTE- 19950607 US/AE-A  
APPLICATION DATA (PATENT)  
{US 477781/95 19950607 [1995US-0477781]}  
- 19950821 US/AS02  
ASSIGNMENT OF ASSIGNOR'S INTEREST  
ADVANCED RISC MACHINES LIMITED FULBOURN ROAD CHERRY HINTON, CAMBRIDGE,  
UNITED KI \* NEVILL, EDWARD COLLES : 19950606  
- 19980526 US/A

PATENT

- 19980908 US/AS01

CHANGE OF NAME

ARM LIMITED FULBOURN ROAD, CHERRY HINTON CAMBRIDGE CBI, ENGLAND 4JN \*

ADVANCED RISC MACHINES LIMITED : 19980521

UP - 2000-08

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<input type="checkbox"/>	L5	l1 and L4	33
<input type="checkbox"/>	L4	(712/209 or 712/210).ccls.	519
<input type="checkbox"/>	L3	l1 near8 interoperab\$	2
<input type="checkbox"/>	L2	L1[ti,ab]	37
<input type="checkbox"/>	L1	(dual or multi or multiple or plural\$) adj2 (instruction adj set)	269

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